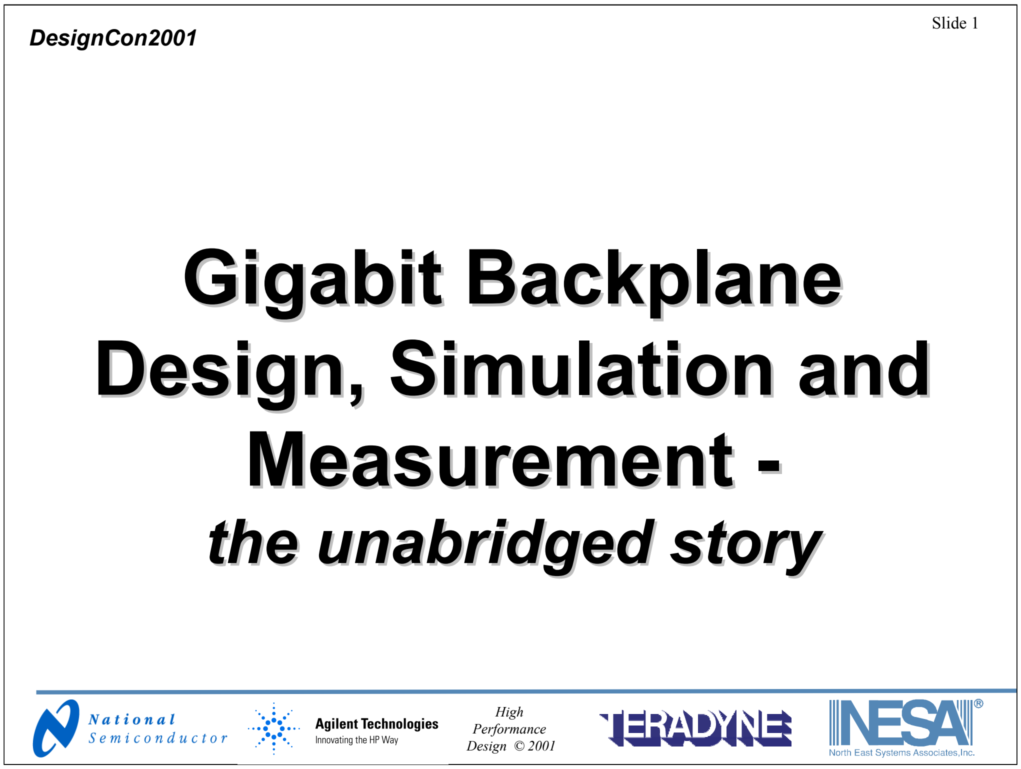

This paper is a joint project between National Semiconductor, North East Systems Associates (NESA), Teradyne and Agilent Technologies on Gigabit backplane design, simulation and measurement.

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Slide 2

Authors

NESA
Dr. Edward Sayre
and
Dr. Jinhua Chen
Mr. Michael Baxter

Teradyne
Mr. Gautam Patel

National Semiconductor
Mr. John Goldie

Agilent Technologies
Mr. Michael J. Resso

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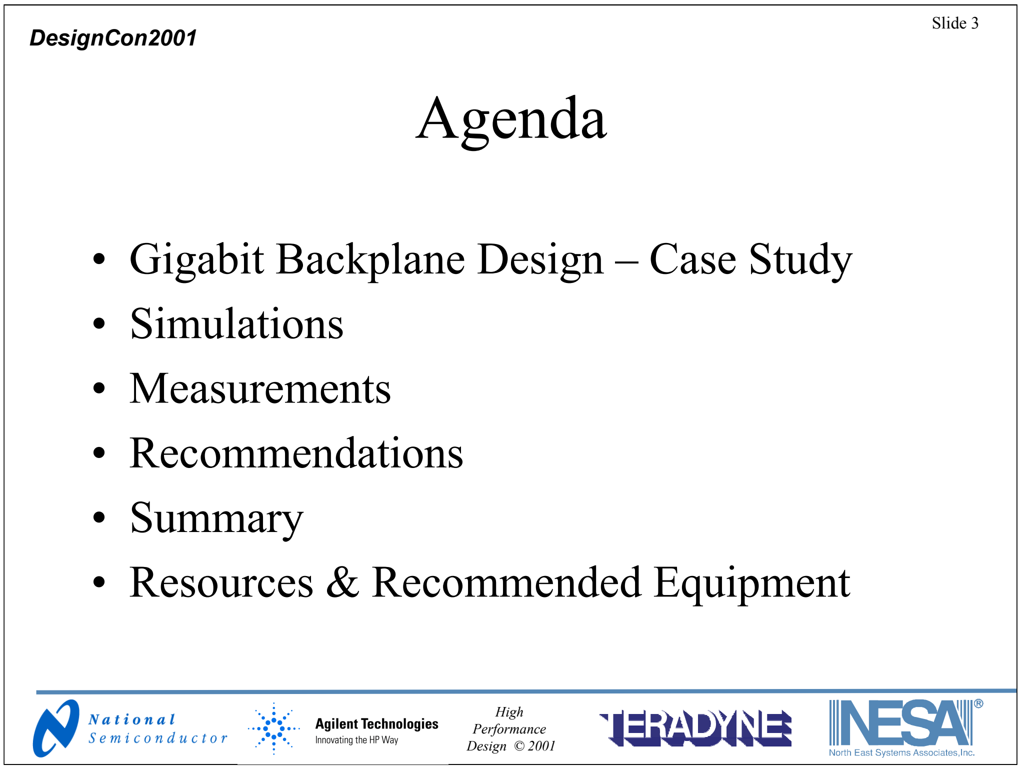
National Semiconductor Corp. - John Goldie – is a graduate of San Francisco State University, holding a Bachelor of Science in Electrical Engineering with a minor in Design & Industry. John joined National Semiconductor's Interface Applications group in 1988. Since then he has worked on LVDS, BLVDS, CML, ECL, GTL, BTL, RS-xxx and other interface technologies. He has also published a number of articles and routinely conducts seminars on Data Transmission topics.

Agilent Technologies - Mike Resso - is a Product Manager in the Lightwave Division of Agilent Technologies. He is responsible for technical training of Agilent field engineers, symposium lecturing and creation of sales tools that will expand the worldwide market growth of high bandwidth oscilloscopes. Mike has over 15 year of experience in the design and development of electro-optic test instrumentation. He has published over 20 technical papers in diverse fields such as infrared detect probe systems, linearly variable optical filters, and electrically conductive antireflection coatings. Mike received his bachelor's degree in Electrical and Computer Engineering from University of California, Santa Barbara.

Teradyne – Gautam Patel - is currently a signal integrity engineer in the New Product Development group. He performs measurements, modeling, and simulation of backplane interconnects. His other functions include applications support, technical presentations and writing of technical papers. Gautam has an MS in Electrical Engineering from Northeastern University.

NESA - Dr. Edward Sayre - 1973 to present; Owner and Director of Engineering of North East Systems Associates, Inc., (NESA). NESA is a high performance engineering and design firm for the computer and communication industries. NESA works with world recognized semiconductor companies to provide interconnect reference designs for their new I/O products. Over fifty systems have been EMC engineered by NESA to pass PCC, Bellcore and CE compliance standards. Dr. Sayre pioneered Time Domain characterization of interconnects as well as proficient use of the better-known frequency domain instrumentation methods.



This paper focuses on high-speed point-to-point links, using LVDS (Low Voltage Differential Signaling) technology across a GTEK based backplane and plug in cards using the VHDM-HSD connector system. Board design, SPICE simulations, and channel performance measurements are discussed in detail. The paper concludes with recommendations to achieve maximum throughput for tomorrow's high performance backplanes operating in the 1-3 Giga bit per second channel speed.

Design

Next is a discussion on the design of the point-to-point Gigabit backplane used as the test bed.

Backplane Design

- Point-to-Point Bus Configuration
- GETEK Backplane with 10” and 20” traces
- GETEK Plug In cards
- VHDM – HSD Connectors
- Gigabit LVDS Driver Test Silicon

The bus configuration is a uncomplicated point-to-point link. Due to the desired high throughput and the required signal edge rate, a multi-drop / multi-point bus configuration was eliminated. The plug in card is connected to the load via a direct connection in the backplane as with in a simple point-to-point link or in a cross bar application.

Material for both the backplane and also the plug in cards was selected to be GETEK over FR4 since the cost differential has lessoned and the GETEK material has become more common in the industry. GETEK offers slightly better high frequency performance and stable performance over temperature. This paper does not compare different materials and their respective performance as that subject has been covered adequately by many other papers to date.

Noting that this is a Gigabit link, the Teradyne VHDM-HSD differential connector was selected.

The LVDS driver and receiver used was test silicon designed by National Semiconductor. The edge rate of this device was targeted for 1.5-2.0 Gbps operation.

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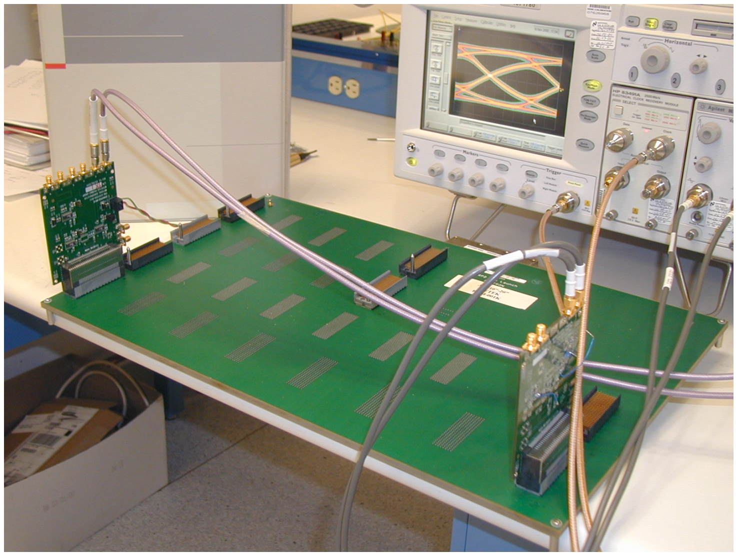
System Picture



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The picture above shows the system under test (SUT) that was the subject of this paper. The backplane was designed by Teradyne and the Plug In cards were designed by National Semiconductor. The backplane provided both 10 inch and 20 inch interconnects.

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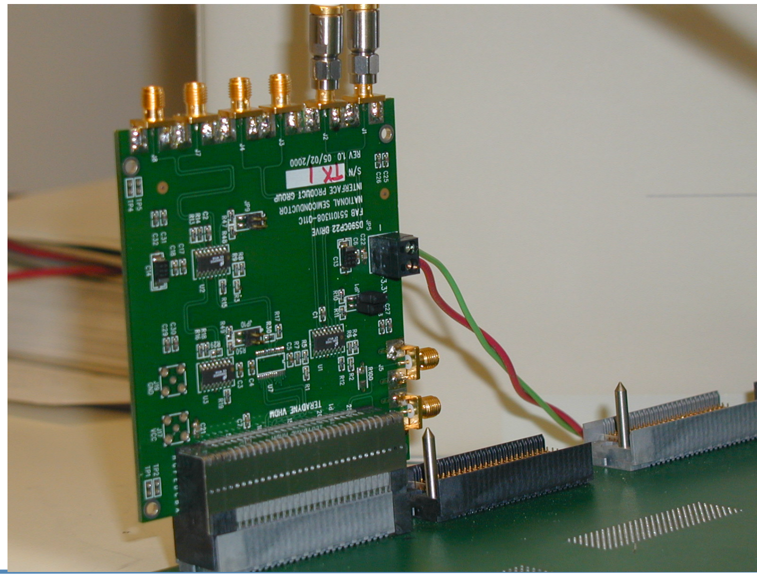
Close Up View of Card & Connector



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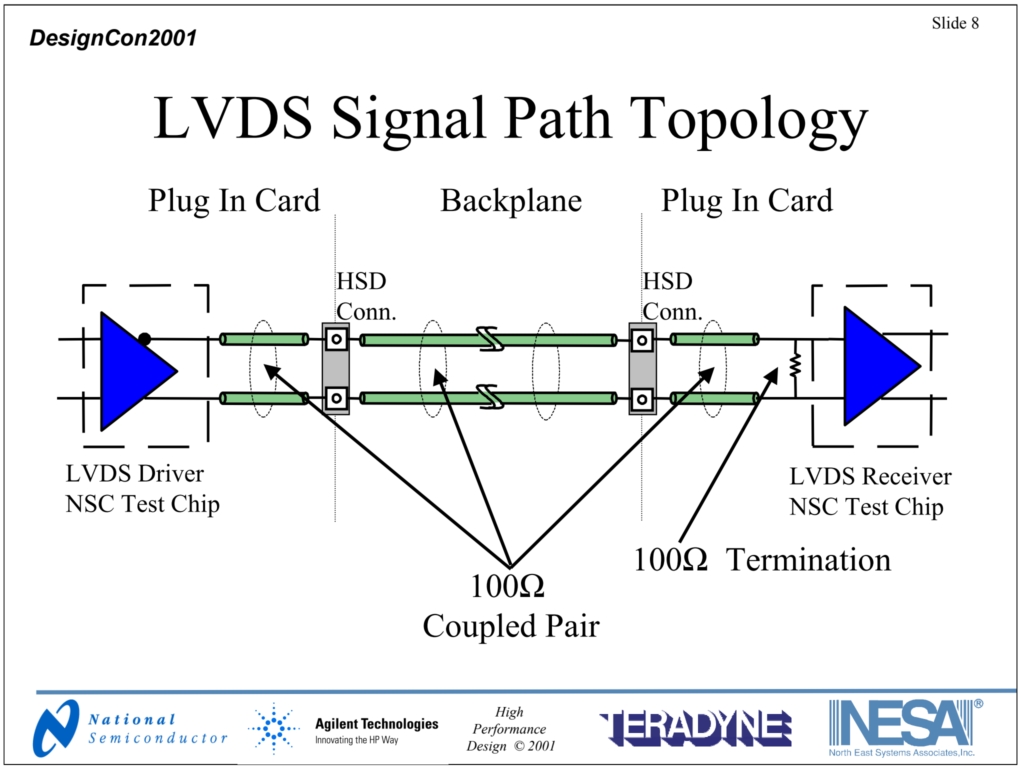
In this close up view of the driver plug in card, the test pair can be seen in the lower right next to the HSD connector. This allowed for test access for the TDR and generator measurements shown later in the presentation. The SMA connectors on the top of the card provided the differential input to the test silicon which was configured as a LVDS line driver and also standard LVDS receiver (without CDR).



The signal path is shown above. This is what is know as a uncomplicated point-to-point link and is optimal for high data rate applications due to the pure and clean signal path.

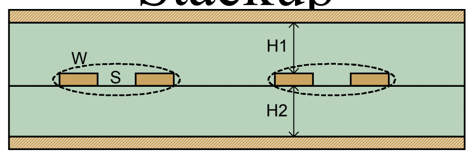
The logic card featured a 2 inch 100 Ohm coupled trace from the LVDS output pads to the HSD connector.

The backplane also used a 100 Ohm coupled pair between connectors. Trace lengths of 10 inches and also 20 inches were available for test.

The plug in card for the load had a 2 inch interconnect to the termination location. A 100 Ohm differential termination resistor was used across the pair and ¼ inch stub connected the LVDS receiver inputs to the line.

Probing of the LVDS signals was done across the 100 Ohm termination and also at the receiver input pins. The NS Test Silicon was packaged in a SOP 14 lead package.

Backplane and Plug In Card Stackup

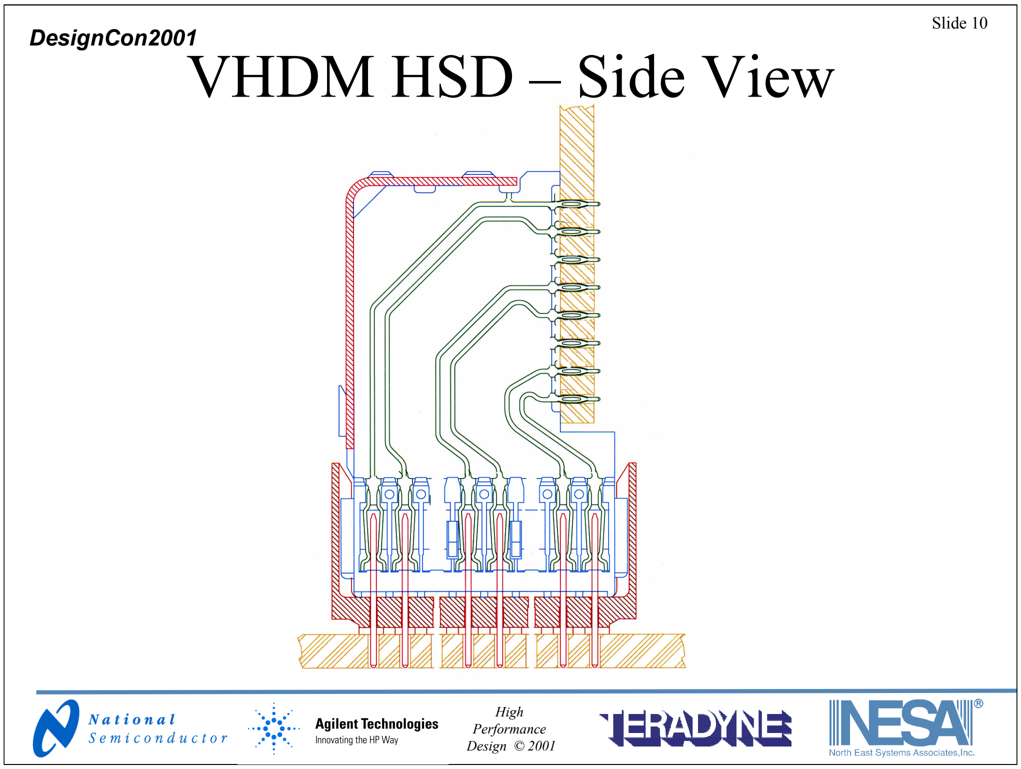


<u>Stackup for the backplane</u>:
H1 = H2 = 10 mils
W = 8 mils
S = 8 mils
Getek material
target differential impedance: 100 Ω
1/2 oz copper

<u>Stackup for the plug in card</u>:
H1 = H2 = 12 mils
W = 8 mils
S = 10 mils
Getek material
target differential impedance: 100 Ω
1 oz copper

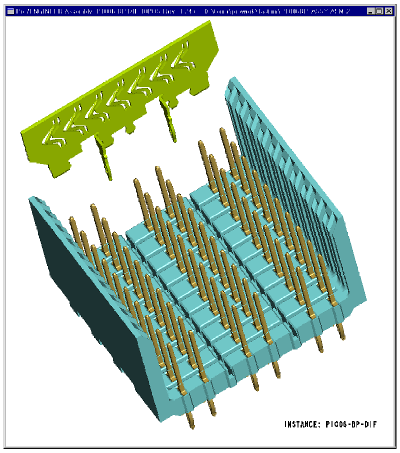
This graphic shows the cross sections of the backplane and also the plug in cards.

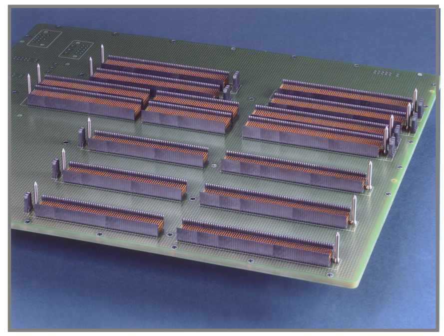
For this project edge-couple differential striplines were chosen. It is not the intention of this paper to compare broadside lines to edge-coupled lines. Edge coupled lines were chosen due to ease of manufacturing and also for routing reasons.



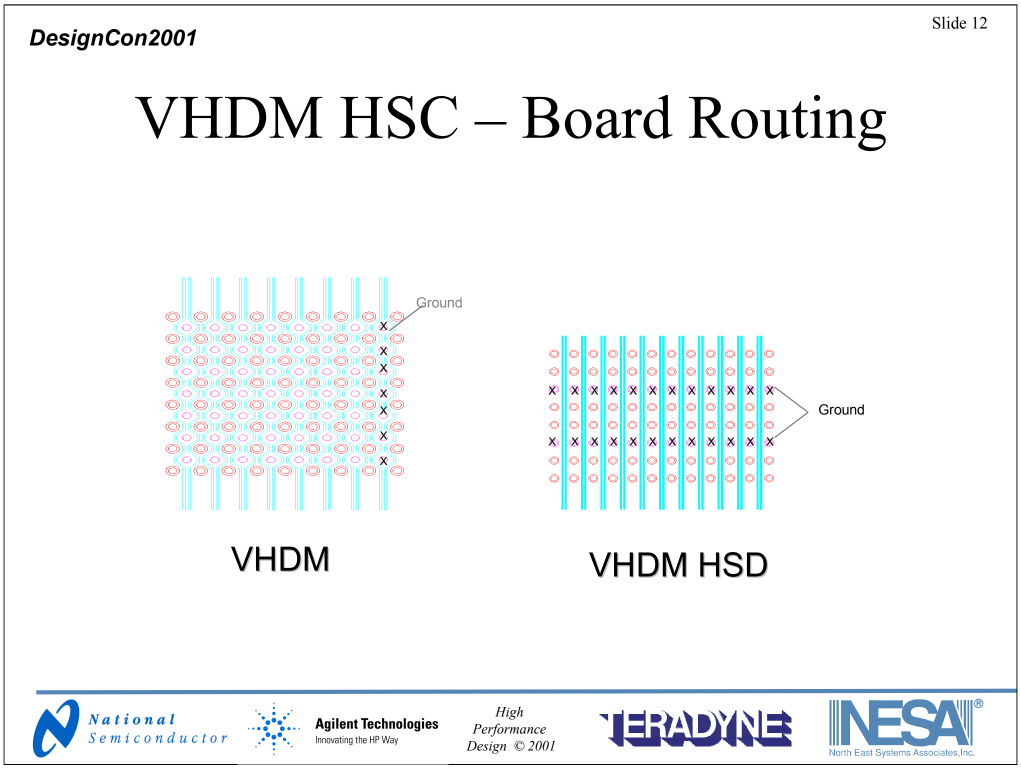
The VHDM-HSD connector was uniquely constructed for differential signal transmission both in the daughtercard and backplane halves. As is shown in the slide above the signal lead frame within the connector is tightly coupled. This was done to minimize the skew within the differential pair. The measured skew within the pairs range from 6 to 10 ps. Also by effectively moving the pairs further apart, the cross talk is greatly reduced. For 200ps edge rates the cross talk ranges from 1.56% to 0.85%. In order to achieve these electrical results density had to be sacrificed, the VHDM 8 row connector has 50 pairs per linear inch where HSD 8 row gives 38 pairs per linear inch.

VHDM HSD – Backplane Shroud

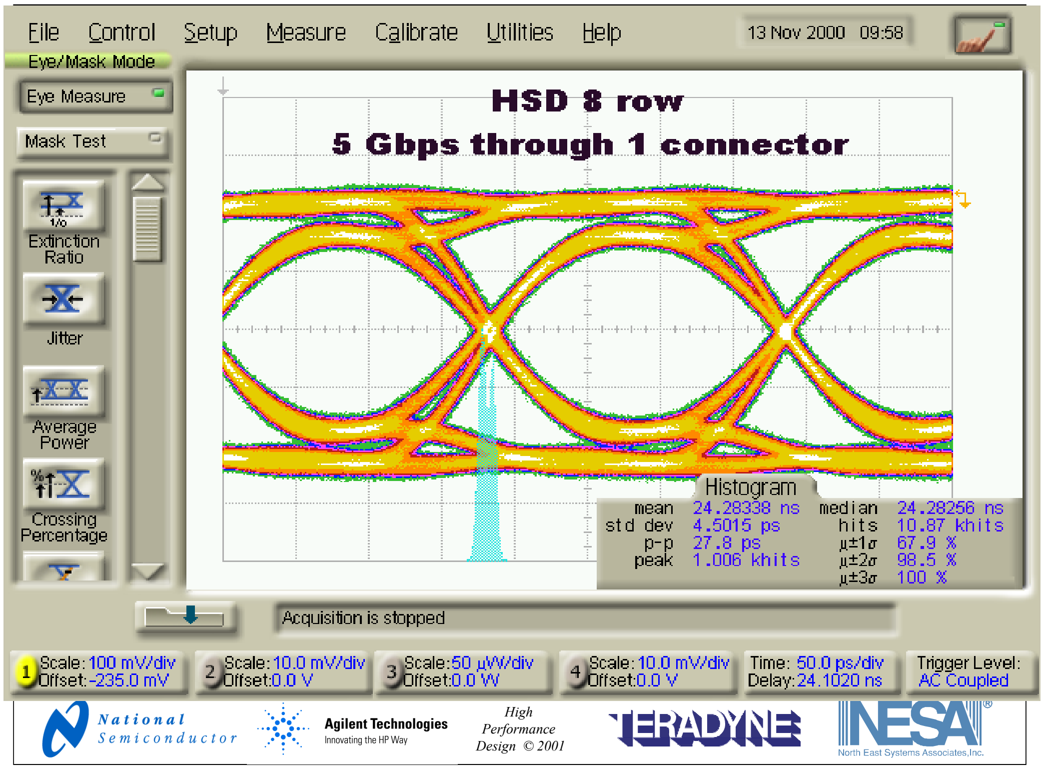




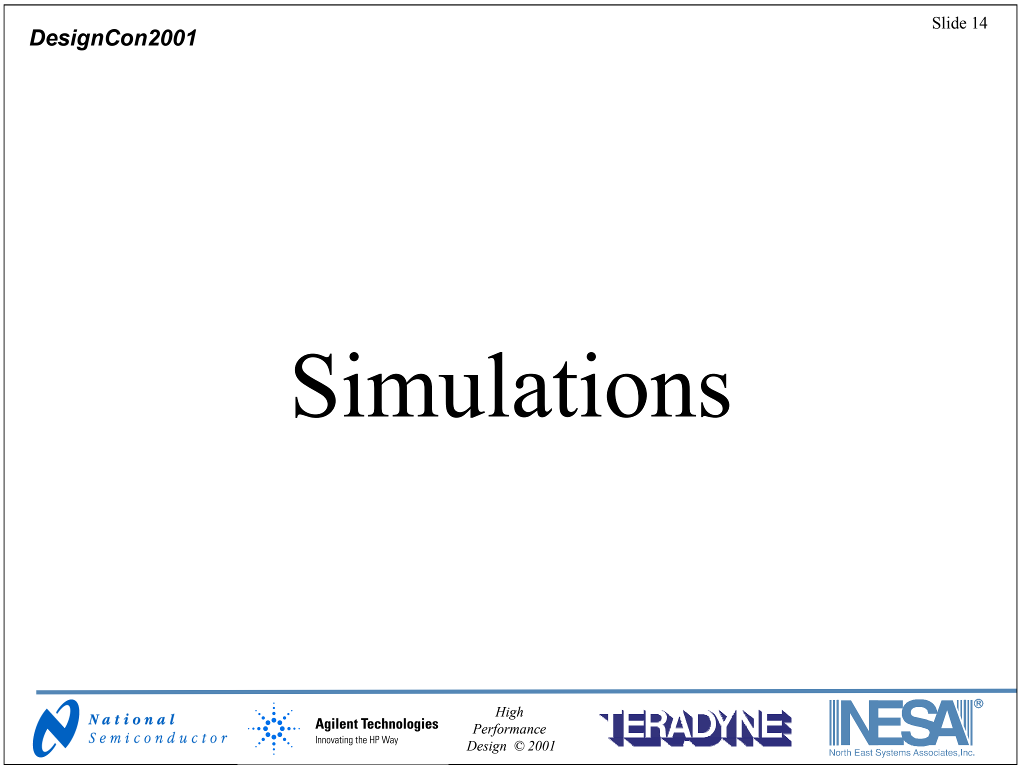
As shown in the previous slide, the daughtercard portion of the connector was optimized for differential signaling. In order to make the entire connector perform well at high speed differential data rates, the backplane module had to be modified as well. This was done by removing 2 signal pins within a column and sliding 2 ground legs in their place (this can be seen in the figure above). The VHDM 8 row connector uses 8 signal pins with 7 ground pins and in the HSD connector 6 signal pins are used with 2 ground pins. The reason that 7 ground pins can be reduced to 2 ground pins is due to the nature of differential signaling.



Another benefit of HSD is in it’s routing. As shown above the VHDM connector, though it offers density , is not ideal for differential signal routing. The HSD connector eliminates the routing bottleneck by moving the interstitial grounds seen in VHDM in line with the signal pins in HSD. This could only be done by the sacrificing of ground pins described earlier. The jogged routing of VHDM effectively adds 23% to the overall trace length. The additional unnecessary trace length can have a severely negative impact at high data rates (>2.5gbs). This is due to the fact that the backplane material becomes very lossy at high frequencies and long lengths.



The figure above shows an eye pattern running at 5 Gbps through a single HSD 8 row connector. The total trace length was 6" in FR4 plus 2' of cable. This figure demonstrates that connector in a stand alone environment performs very well at 5 Gbps. The problem arises when the same data rate is passed through a more realistic system which includes 2 connectors plus some trace length . In this environment the effects of the dielectric become the dominant factor.



The next phase the the project was to look at the simulations of the system. Simulations were completed by NESA for both impedance and wave shape using Avanti Corp.'s Star-Hspice analog circuit simulator

The simulated interconnect included the two test cards and the backplane, which were connected with two Teradyne HSD backplane connectors.

The cards and backplane were fabricated with GETEK dielectric material. HSpice lossy W-element models (with NESA-supplied parameters) were used for the transmission line models.

Both differential TDR profiles and eye patterns are presented in the following slides. The backplane length was set to 10" and 20" and data rates of 1.5 Gbps, 2 Gbps and 2.5 Gbps were simulated using the K28.5 data pattern.

Note: additional via capacitances were included in the simulations as needed. Card via capacitance, cvia = 1 pF; backplane via capacitance, bvia = 2 pF

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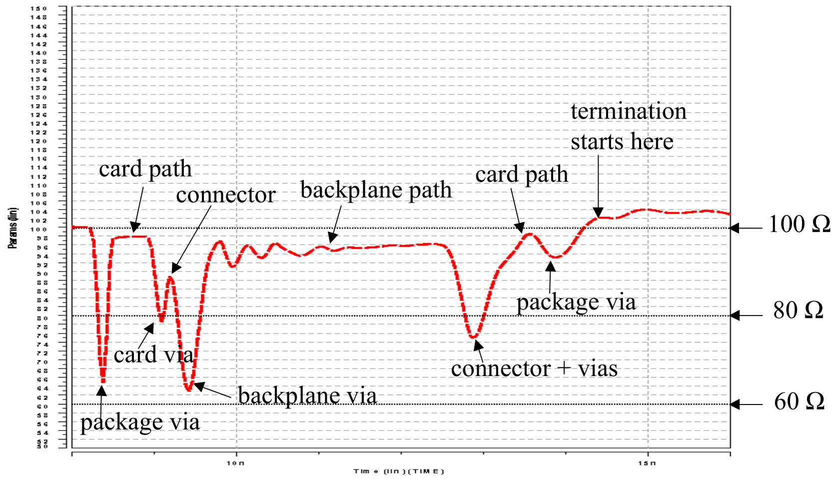
Differential TDR Simulation w/ 100 ps TDR Rise Time

(2 - 2" cards + 10" backplane + 2 HSD connectors)



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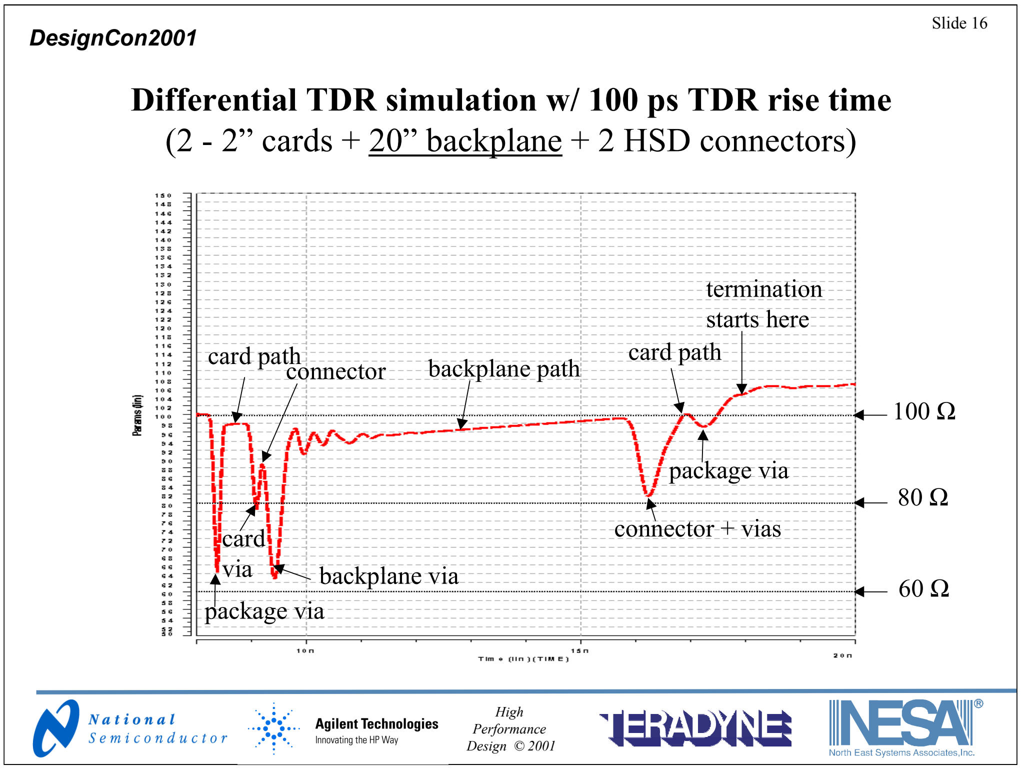
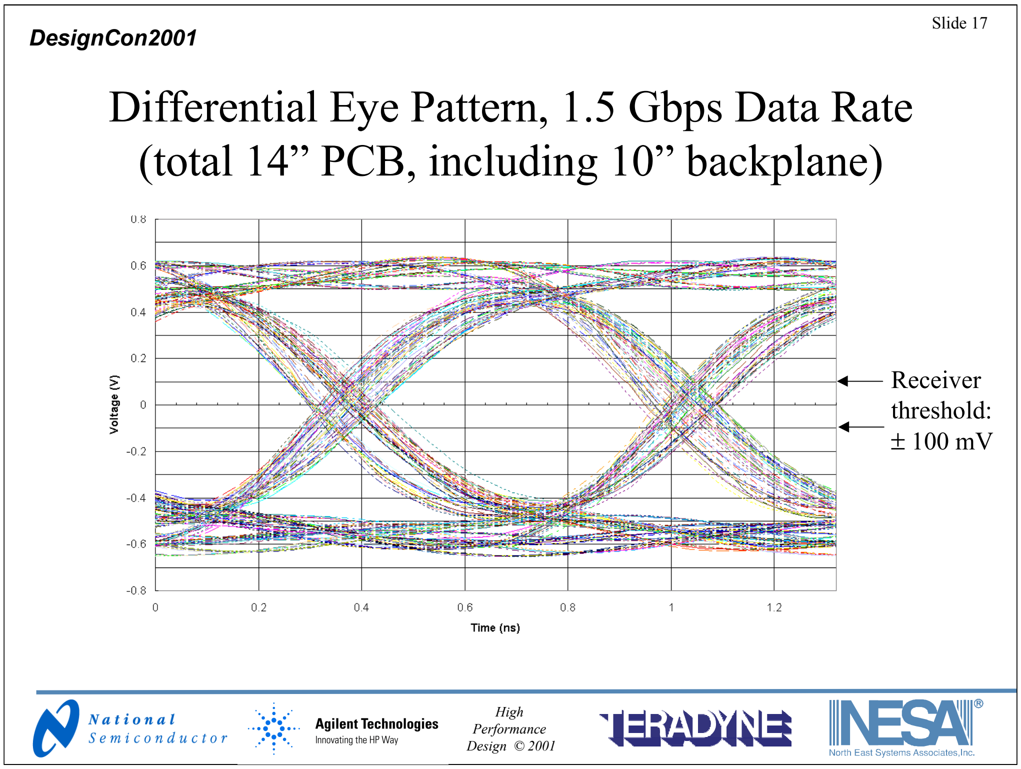
The TDR for a short path shows the effects of the discontinuities suffered by a waveform traversing the semiconductor package, the logic card paths, backplane connectors to the matched 100 Ohm termination. Note that the card via is generally a lesser effect that the backplane via due to the relative differences in thickness between the two. The slight rise in the TDR impedance on the backplane is due to the series resistance of the etch. As the signal waveform travels through the connector, it suffers some reflections shown as ripples in the TDR. The discontinuity of the second connector is substantially less due to the loss in risetime suffered by the waveform due to dielectric losses. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

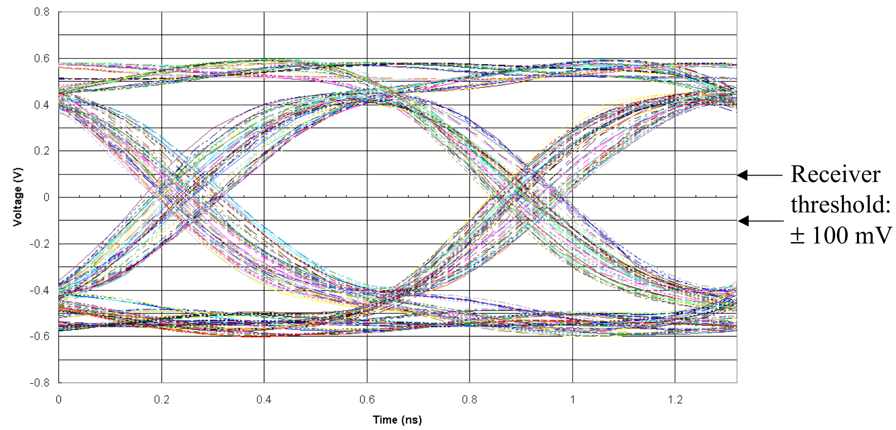


The TDR for a longer path shows similar effects of the discontinuities suffered by a waveform traversing the semiconductor package, the logic card paths, backplane connectors to the matched 100 Ohm termination. Note that the card via is generally a lesser effect that the backplane via due to the relative differences in thickness between the two. The more pronounced rise in the TDR impedance on the backplane is due to the longer path series resistance of the etch. Similar reflections, shown as ripples in the TDR occur at the near end connector, but are largely missing after the second. The discontinuity of the second connector is even less than that exhibited over the shorter path due to the greater loss in risetime suffered by the waveform. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

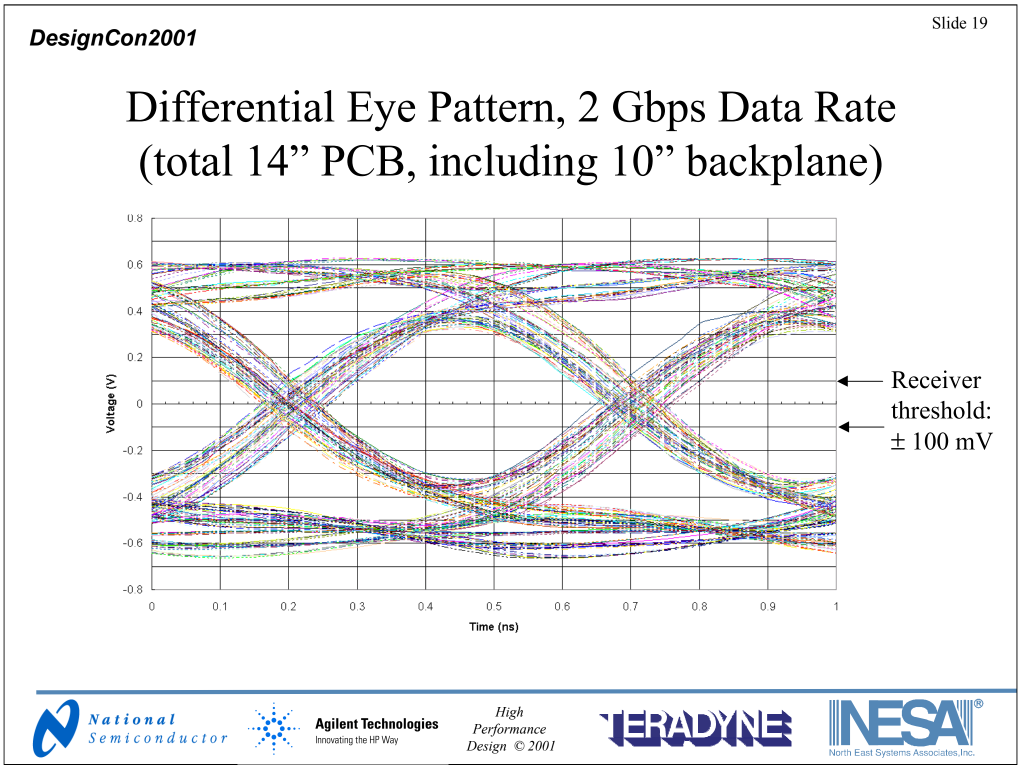


This eye diagram of a 1.5 Gbps data rate over a 10" backplane shows that the voltage margin for this path is more than satisfactory and is approximately 320 mV above the specified differential LVDS thresholds. The time jitter through the short backplane path is on the order of 160 ps. The attenuation of single bits is only slightly greater than bit patterns where the peak voltage excursion has been reached indicating that the principal loss mechanism is high frequency in nature. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

Differential Eye Pattern, 1.5 Gbps Data Rate (total 24” PCB, including 20” backplane)



This eye diagram of a 1.5 Gbps data rate over a 20” backplane shows that the voltage margin for this path is more than satisfactory and is approximately 300 mV above the specified differential LVDS thresholds. The time jitter through the short backplane path is on the order of 180 ps. The attenuation of single bits is somewhat greater than bit patterns across a 10” backplane. This indicates that the principal loss mechanism is high frequency in nature and not DC or skin effect etch loss. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.



This eye diagram of a 2.0 Gbps data rate over a 10" backplane shows that the voltage margin for this path is less satisfactory than at 1.5 Gbps and is approximately 210 mV above the specified differential LVDS thresholds. The path should work satisfactorily. The time jitter through the short backplane path is on the order of 120 ps. The attenuation of single bits is only somewhat greater than bit patterns at 1.5 Gbps indicating that the principal loss mechanism is high frequency in nature. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

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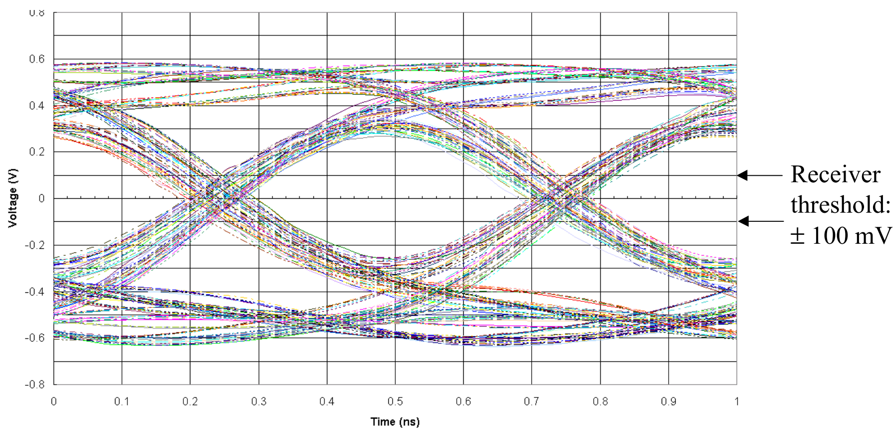
Differential Eye Pattern, 2 Gbps Data Rate (total 24” PCB, including 20” backplane)



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This eye diagram of a 2.0 Gbps data rate over a 20” backplane shows that the voltage margin for this path is less satisfactory than at 1.5 Gbps and is approximately 180 mV above the specified differential LVDS thresholds. The path should work satisfactorily. The time jitter through the short backplane path is still on the order of 120 ps. The attenuation of single bits is somewhat greater than bit patterns at 1.5 Gbps indicating that the principal loss mechanism is high frequency in nature. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

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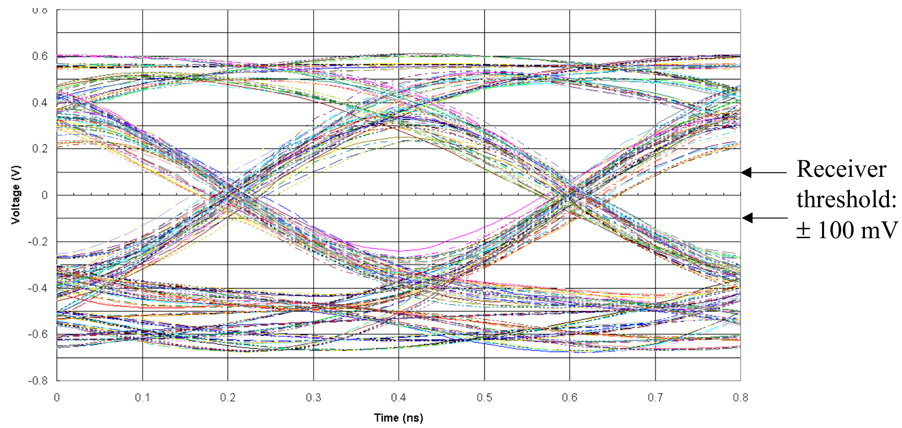
Differential Eye Pattern, 2.5 Gbps Data Rate (total 14” PCB, including 10” backplane)



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This eye diagram of a 2.5 Gbps data rate over a 10” backplane shows that the voltage margin for this path is less satisfactory than at 2.0 Gbps and is approximately 120 mV above the specified differential LVDS thresholds. The path should work satisfactorily. The time jitter through the short backplane path is still on the order of 110 ps. The attenuation of single bits is greater than bit patterns at 2.0 Gbps indicating that the principal loss mechanism is high frequency in nature. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.

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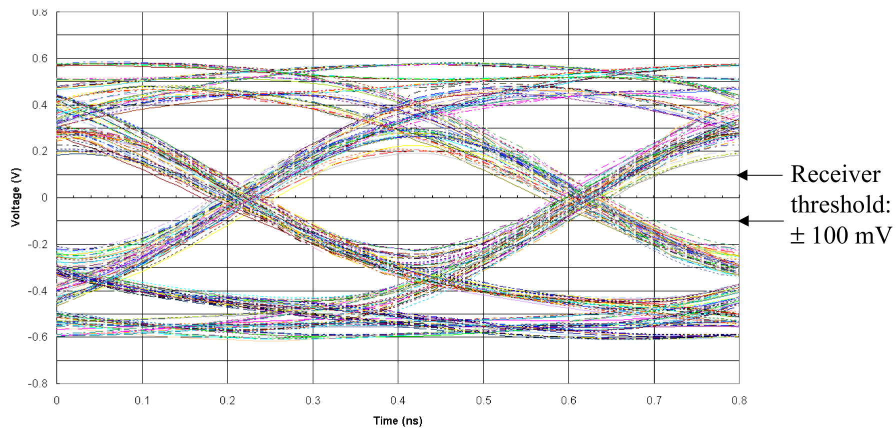
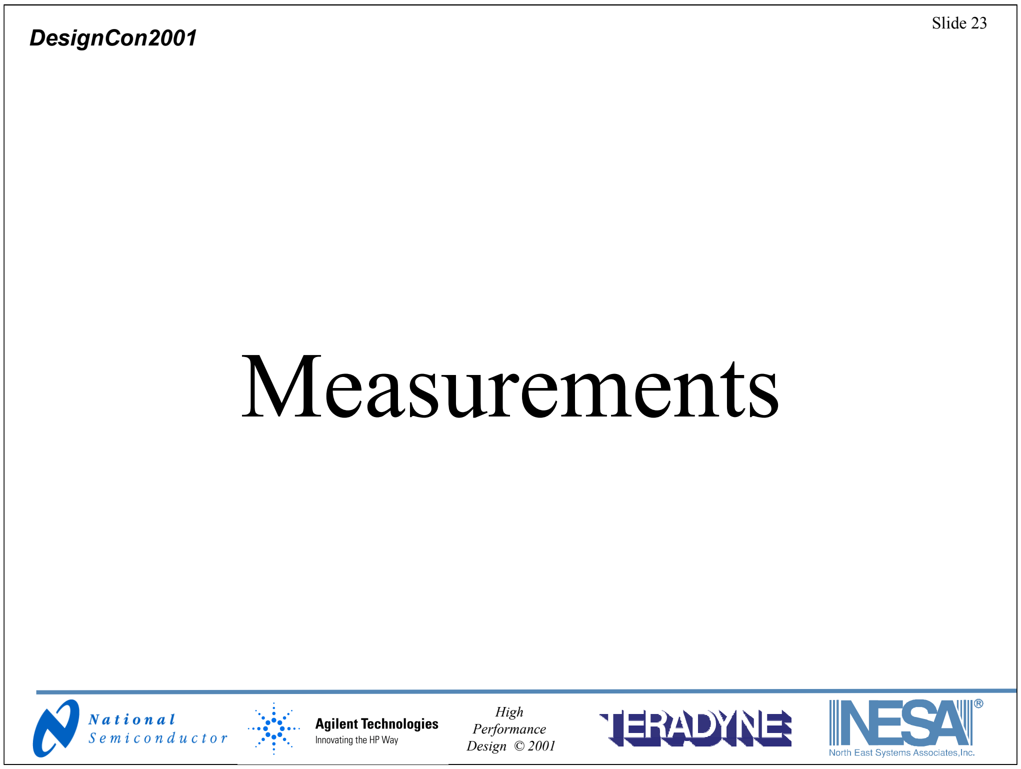
Differential Eye Pattern, 2.5 Gbps Data Rate (total 24” PCB, including 20” backplane)



This eye diagram of a 2.5 Gbps data rate over a 20” backplane shows that the voltage margin for this path is less satisfactory than for the 10” backplane at 2.5 Gbps and is approximately 100 mV above the specified differential LVDS thresholds. The path should work satisfactorily, especially if the real thresholds are less than 100 mV. The time jitter through the short backplane path is still on the order of 100 ps. The attenuation of single bits is greater than bit patterns at 2.0 Gbps. Double bit effects are also apparent indicating that the principal loss mechanism is high frequency in nature. The via capacitances that were included in the simulations are - Card via capacitance: cvia = 1 pF; backplane via capacitance, bvia = 2 pF.



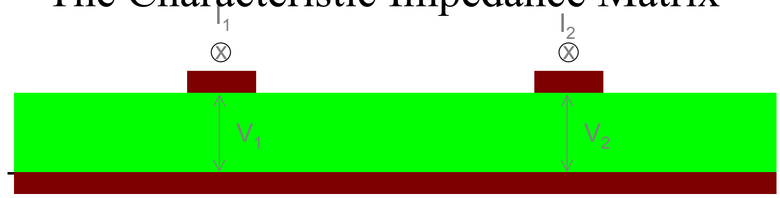
The final phase of the project was to check predictions and simulations against actual bench measurements. For this, a variety of Agilent equipment was used to make TDR and wave shape measurements.

Connection to the test equipment was done with 50 Ohm coax cables and edge launch SMA connectors.

Probing of the LVDS signals was done with a passive divider and biasing circuit to allow for a connection to high bandwidth 50 Ohm scope channels.

Baseline measurements of the equipment were taken along with channel measurements. These are discussed on the following slides.

Differential Impedance:
The Characteristic Impedance Matrix



$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{22}I_2 + Z_{21}I_1$$

Example:
Characteristic Impedance Matrix [ohms]:

	1	2
1	**49.6**	**6.4**
2	**6.4**	**49.6**

Coupling Factor (6.4)
Self Impedance (49.6)

If there were no coupling between transmission lines, the impedance of a line, as defined by the ratio of the voltage across the paths and the current through them, would be dependent on just the line parameters of the one line. However, as soon as coupling is introduced, the voltage on one line may be dependent on the current in an adjacent line. To include these effects, the concept of impedance or characteristic impedance must be expanded to allow for one trace interacting with another. This is handled by expanding the impedance into an impedance matrix.

Any two transmission lines, each with a signal path and a return path, can be modeled using an impedance matrix. The diagonal terms are the impedance of the line when there is no current in the adjacent line. This is sometimes called the self impedance. The off diagonal elements represent the amount of voltage noise induced on the adjacent trace when current flows on the active line. If there were little or no coupling, the off diagonal impedance would be near zero.

As the coupling between the lines increase, the off diagonal terms will increase. For example, if the microstrip traces, as illustrated above, were moved closer together, the diagonal impedance would not change very much, but the off diagonal terms would increase.

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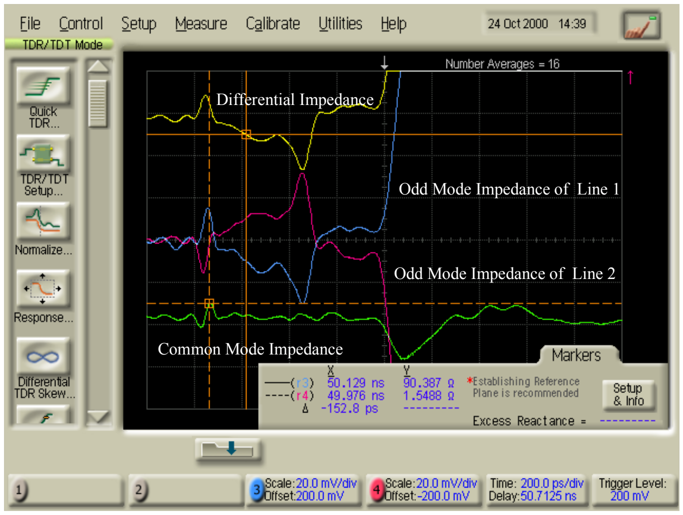
Differential & Common Mode Impedance of the Backplane



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The TDR instrument set upstate for the top three measurements on the TDR display is as follows: TDR step generators are in differential stimulus state. This means the two TDR steps being launched into the backplane are of equal and opposite polarity. The steps are 40 picosecond risetime with 200 (and -200 millivolts) amplitude. The top yellow waveform is the differential impedance, defined as channel 1 - channel 2. Since the stimulus is differential, channel 1 - (- channel 2) is actually channel 1 + channel 2. Thus, the differential impedance measurement is made by placing the marker on this waveform near the middle of the backplane path and noted as 90.39 ohms.

The two middle waveforms are the odd mode impedance of each of the differential lines (red and blue). TDR stimulus is still differential. This measurement is made by selecting channel 1 or channel 2 as the marker reference channel and reading directly from the marker tab in the lower right portion of the screen.

The bottom green waveform is the common mode impedance. The TDR stimulus for this measurement has been changed to common mode drive (in-phase and driven on each line of the pair). This TDR configuration yields common mode stimulus and differential response (mixed mode analysis). The result is channel 1 - (+ channel 2). This measurement is made by placing the marker on this waveform near the connector and can be read as 1.55 ohms.

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Definition of Odd and Even Mode Impedance

(Special case: symmetric)

$$V_{odd} = \frac{1}{2}(V_1 - V_2) \qquad Z_{odd} = \left.\frac{V_{odd}}{I_1}\right|_{V_{even}=0}$$

$$V_{even} = \frac{1}{2}(V_1 + V_2) \qquad Z_{even} = \left.\frac{V_{even}}{I_1}\right|_{V_{odd}=0}$$

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Based on the definition of the impedance matrix, and the definition of odd and even mode, the impedance of each mode can be calculated. The odd mode impedance is the impedance a driver would see, looking into one of the lines, when the pair of lines is driven in the odd mode, or with a differential signal. Likewise, the even mode impedance is the impedance a driver would see, looking into one of the lines, when the pair of lines is driven in the even mode, or by a common signal.

If there were no coupling, both the odd and even mode impedances would be equal, and equal to the impedance of just one isolated line, as expected. However, with coupling, there are additional current paths between the signal lines in odd mode, and the odd mode impedance decreases. Some current will flow not only from the first signal line to the return path, but through to the second signal line and then into the return path. This increased current through the coupling path results in a decrease in the odd mode impedance of one line with increasing coupling.

The even mode is also affected by the coupling. When driven with a common signal, there is no voltage difference between the two signal traces. There is thus no coupled current between the signal lines and the even mode impedance is higher than the odd mode.

A universal equation for a directional coupler contains a coefficient of coupling, k, defined as the ratio of the difference, Zoe-Zoo to the sum, Zoe+Zoo, of the even and odd mode characteristic impedances. The over-all characteristic impedance is equal to the square root of the product of the even and odd mode characteristic impedances, Zo^2=Zoe x Zoo. These two equations are thus used to calculate the even and odd mode impedances for the desired coupling and over-all Zo.

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Even and Odd Mode Impedance of LVDS Backplane

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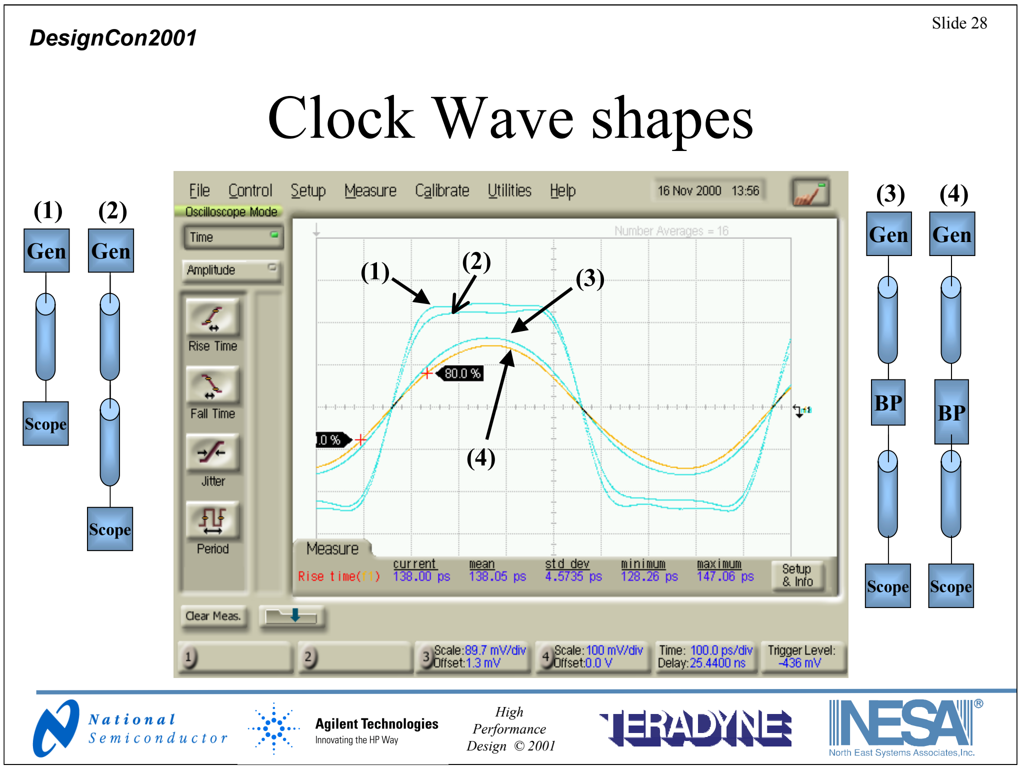
The even and odd mode impedance measurements can be made by selecting only one of the differential lines and changing the TDR step stimulus from differential mode to common mode drive. This is simply changing from equal and opposite polarity steps to equal and same polarity steps, respectively. Waveform memory was implemented to first store the odd mode impedance, then stimulus was changed to common mode and the even mode impedance was obtained. The vertical separation of the even and odd mode impedance waveforms on the display of the TDR is exhibiting the phenomena of good differential coupling.

A more subtle waveform is shown in between the even and odd mode waveforms. This is the self impedance of the one differential line. This measurement is obtained by selecting a single-ended TDR stimulus and not driving the second differential line at all.



Four wave forms are show above. From the signal with the fastest rise time to the slowest:

(1) The signal with the fastest rise time is the generator connected directly to the scope via a 50 Ohm coax cable.

(2) The signal with the next fastest rise time is the generator connected directly to the scope via two 50 Ohm coax cables connected in series.

(3) The next fastest signal is the clock signal passing through the 10 inch backplane interconnect.

(4) The slowest signal is the clock signal passing through the 20 inch backplane interconnect.

The bandwidth of the backplane filters the signal and causes rise time degradation and attenuation. The 10+ inch interconnect increased the rise time by 80-100 ps and the 20+ inch interconnect increased the rise time by about 120ps.

Note that the time base is 100ps/div.

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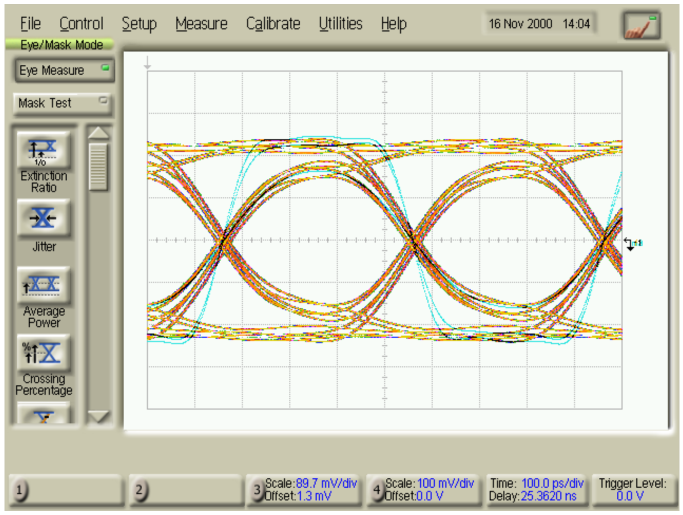
Slide 29

K28.5 Eye Pattern (14”)



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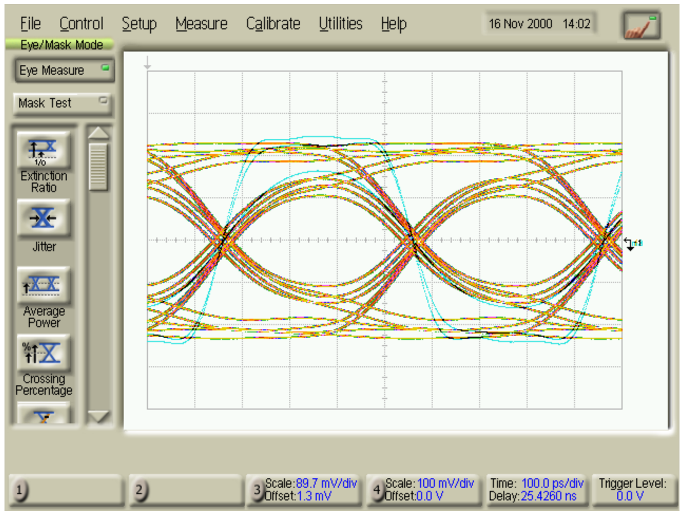
The K28.5 pattern is driven across the backplane from the signal generator to the scope in the same configuration as in test case #3 on the prior slide. Also shown are the three clock wave shapes for comparison. The K28.5 pattern has five rising edges and 5 falling edges which can be seen in the scope shot above. The data rate is 2.5Gbps and a differential waveform is shown. The bandwidth ISI (Inter Symbol Interference) can be seen here in the form of increased jitter at the zero crossing. If the prior data bit was in the same state the line charges to a higher value, this when the transition occurs there is a different starting point compared to that of a bit that had just switched to that state. The result is increased deterministic jitter as shown above. This plot should also be compared to that of a PRBS pattern which is worse case. The PRBS pattern does not force transitions to occur, in fact it includes long strings of 1s and 0s which fully charge the line. This is the benefit of encoding of data. An example of encoding is the popular 8b/10b code that guarantees transitions and DC balancing of the data on the line which improves the eye opening and thus reduces jitter. The K28.5 pattern is commonly used to represent the worse case pattern as it includes the highest and lowest frequency patterns of 8b/10b.

K28.5 Eye Pattern (20")



The loading effect of the backplane can be seen even clearer in this scope shot. The interconnect was changed from the 10 inch backplane path to the 20 inch path. With the longer length, the loading effects are greater, and they are easier to see. Note that on the longer path, the rise time is slowed further, thus a drop in amplitude occurs and the eye closes down further.

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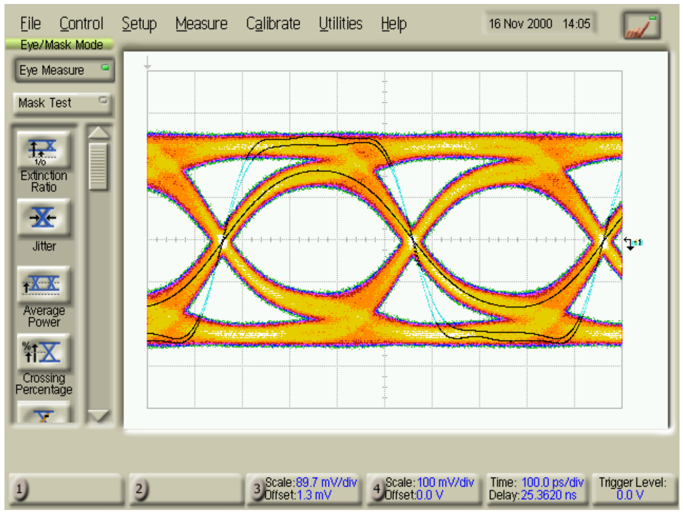
PRBS-31 Eye Pattern 10”



This scope scope is the same as the K.28 patter shown on slide #27 except the pattern has been changed to PRBS-31. The impact is more jitter at the zero crossing point and also a wider distribution at the top and bottom base lines.

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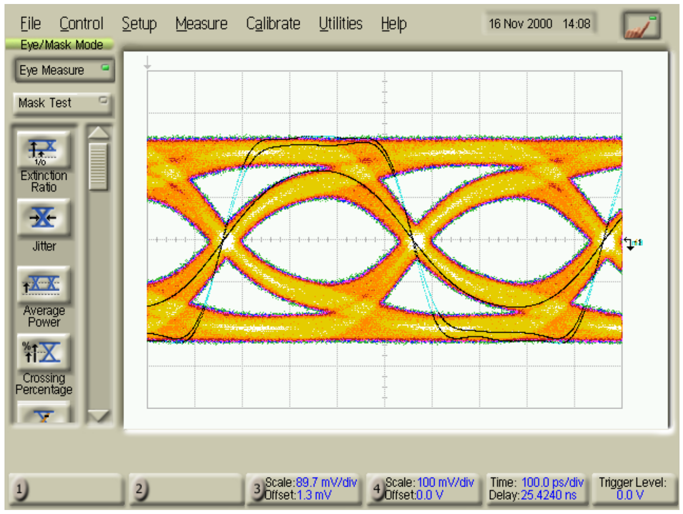
PRBS-31 Eye Pattern 20”



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This scope scope is the same as the K.28 patter shown on slide #28 except the pattern has been changed to PRBS-31. The impact is again more jitter at the zero crossing point, and further closing of the amplitude of the signal at the center of the eye pattern due to the slower edge.

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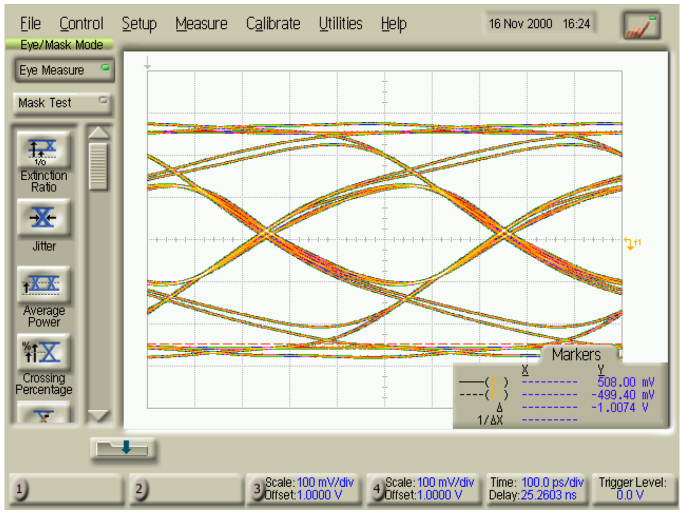
Slide 33

LVDS Driver - 10”/2Gbps/K28



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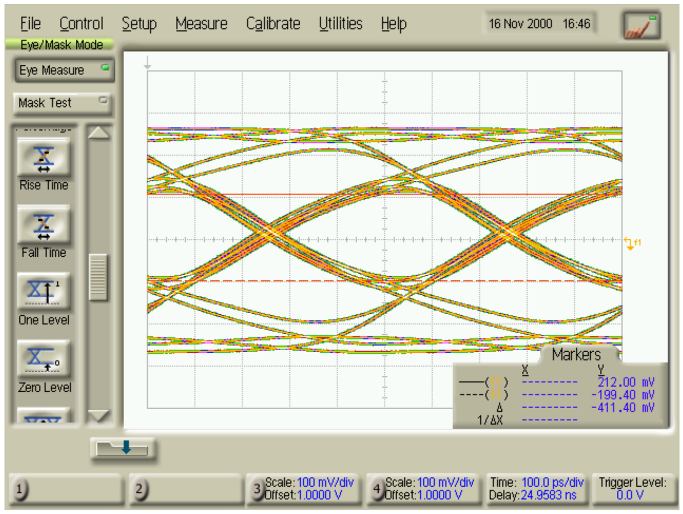
This scope shot uses the National test silicon LVDS driver. A complicated passive load has been used to allow direct measurement of the LVDS driver into the 50 Ohm on the receiver card in place of the LVDS receiver. This allows the signal quality to be checked at the receiver input pads. This divider provides an equal vent 100 Ohm load to the driver and also a 2:1 divider to the scope. Some additional rise time degradation is induced by this probing method thus the amplitude is reduced further. This can be seen when comparing this scope shot to the simulation eye pattern.

Even though the eye is closing down, the design of the receiver and CDR circuitry will recover the data. The LVDS receivers tend to have very tight thresholds can switch with as small as 10mV signal amplitudes. CDR circuitry depending upon implementation tends to be able to recover data from a signal with jitter up to 50-70% of the unit interval.

LVDS Driver - 20”/2Gbps/K28



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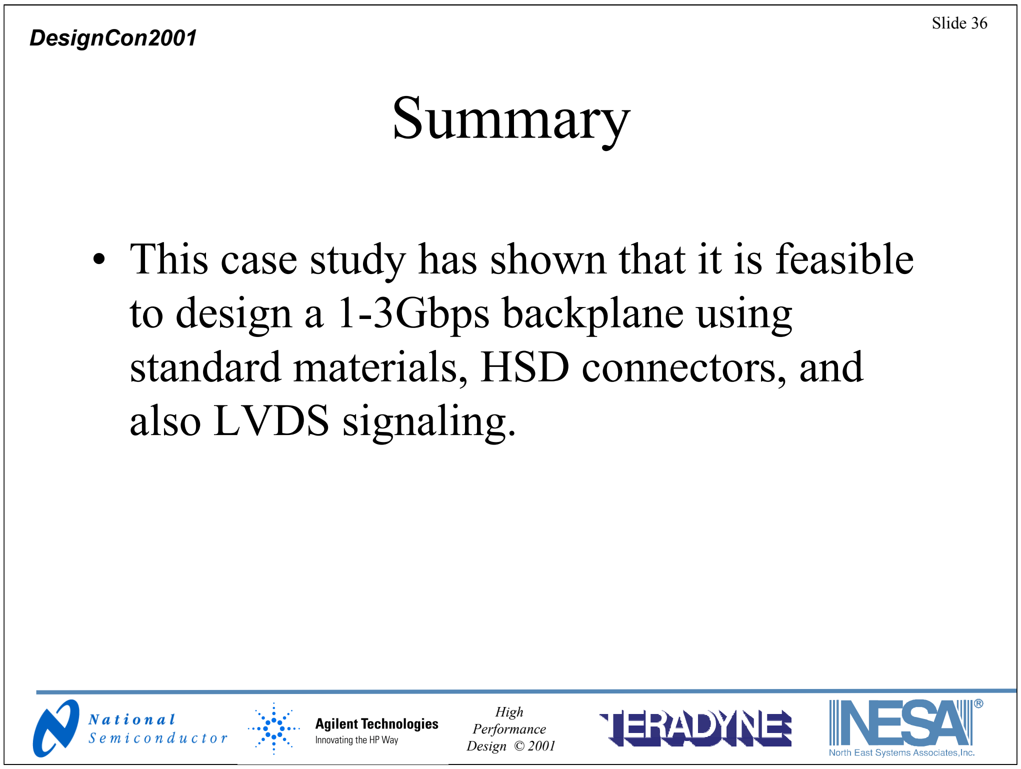
This scope shot shows the additional loading effects of the longer backplane interconnect. Once again this is illustrated by the reduced amplitude and also the increased jitter.

Recommendations

- Optimized interconnect for best differential signal transmission:
  - Limit the number of VIA on the line
  - Match Impedance and trace length, maintain balance of pair
  - Proper termination is required
  - Keep stubs as short as possible
- Predict and verify signal quality - Evaluate eye patterns at the load for signal quality
- Signal edge rates quicker than 500ps should be used in point-to-point links only
- For 200 ps signal edge rates, equipment should have a rise time of 100ps for < 10 % error, and 29 ps for < 1% error

This slide provides recommendations for the design and evaluation of backplane Giga bit links.

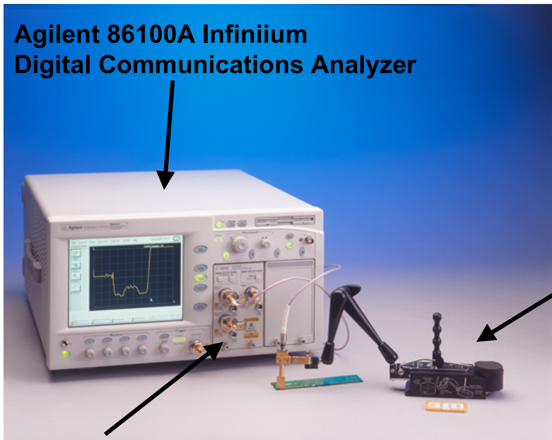


This case study has shown that it is feasible to design a 1-3Gbps backplane using standard materials, VHDM HSD connectors, and employing LVDS signaling.

Additional enhancements to the LVDS driver to speed up the test silicon's driver edge rate will allow for operation at 2.5 / 3.125 Gbps. Above these rates additional tuning of the backplane would be required to address the interconnect's bandwidth.

The TDR plots provide great insight into the interconnect to determine which structures impact the signal path. Analyzing the signal quality at the load gives a good indication of the bandwidth of the interconnect and also the amount of jitter.

Bench Equipment



Terminology

TDR: Time Domain Reflection
TDT: Time Domain Transmission
DTDR: Differential TDR
DTDT: Differential TDT

Agilent N1020A TDR Probe

Agilent 83484A
2 Channel 50 GHz Module
(not shown)

Agilent 54754A
Differential TDR Module
Two independent TDR channels

This slide shows the test equipment used for the bench measurements.

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Slide 38

Resources

- Simulation and Platform Design Services
  www.nesa.com
- LVDS Semiconductors
  www.national.com/appinfo/lvds
- Differential Connectors
  www.teradyne.com/prods/bps/home.html
- Signal Integrity Test Equipment
  www.agilent.com/comms/tdr

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The slide above provides links to web sites that include additional information on the topics presented in this paper.

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Demos

The Backplane is on display in the National Semiconductor booth.

Test Equipment used in this paper is on display in the National and Agilent booths.

The VHDM-HSD connectors are on display in the Teradyne booth.

Simulation Information is available in the NESA booth.

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(fax) (886-2) 2545-6723

Other Asia Pacific Countries:
(tel) (65) 375-8100
(fax) (65) 836-0252
Email: tm_asia@agilent.com

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